

Fig. 1

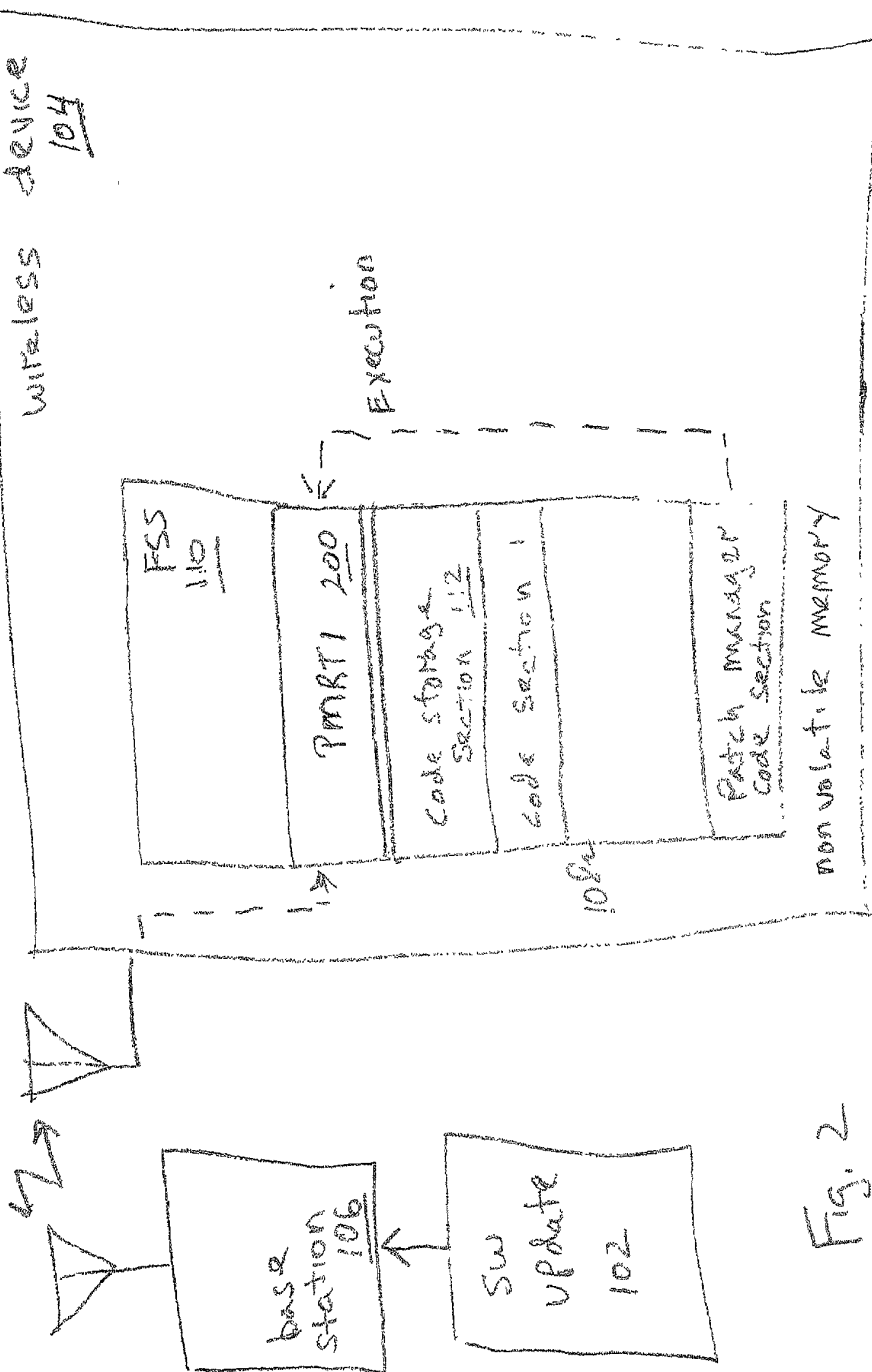
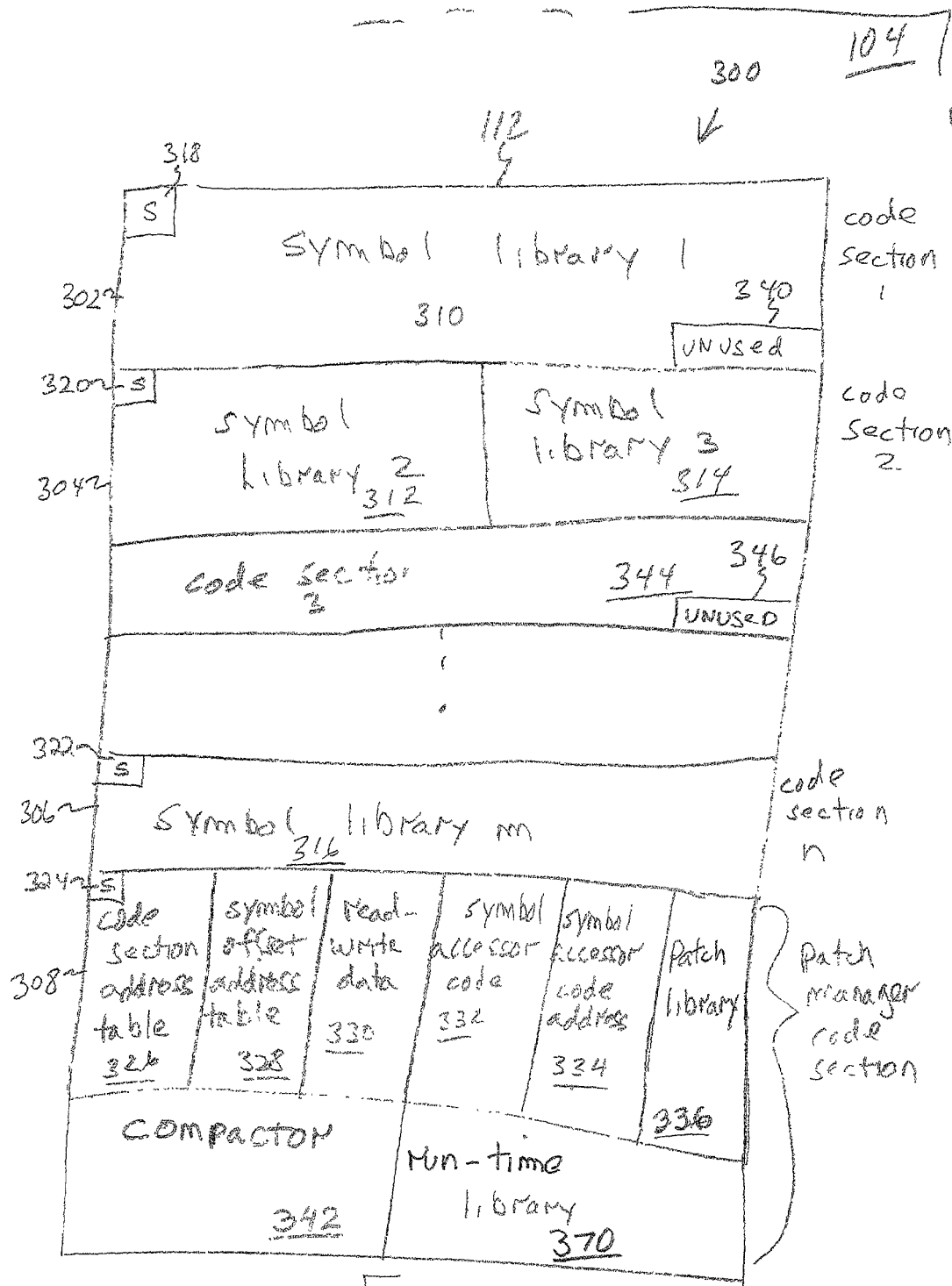


Fig. 2



The diagram illustrates a memory layout with several blocks and sections. On the left, a vertical stack of memory blocks is shown, each with an address and a pointer to a section:

- 1st memory block 400 → points to Code section 1 302
- 2nd memory block 402 → points to Code section 2 304
- 3rd memory block 404 → points to Code section 3 344
- 4th memory block 406 → points to Patch manager code section 308

At the top, a large section is labeled "System data code section 472". Below it, a dashed line separates a section labeled "1st PMRTI 454" from "Code section 474". Further down, a section labeled "470 Dynamic instruction set" is shown. Below that, a section labeled "452 updated Patch manager code section" is shown. At the bottom, a section labeled "450 new code section n" is shown.

On the right side, two large curly braces group the sections:

- Brace 110 groups the sections from "1st PMRTI 454" down to "450 new code section n".
- Brace 112 groups the sections from "Code section 1 302" down to "Patch manager code section 308".

Fig. 4

Symbol offset address table		
Symbol ID	code section ID	Offset
X-1	CS-1	03
Y-1	CS-1	15
P-1	CS-2	11
Q-1	CS-2	33
AA-3	CS-2	47
⋮		

Fig. 7

TOP SECRET 06001

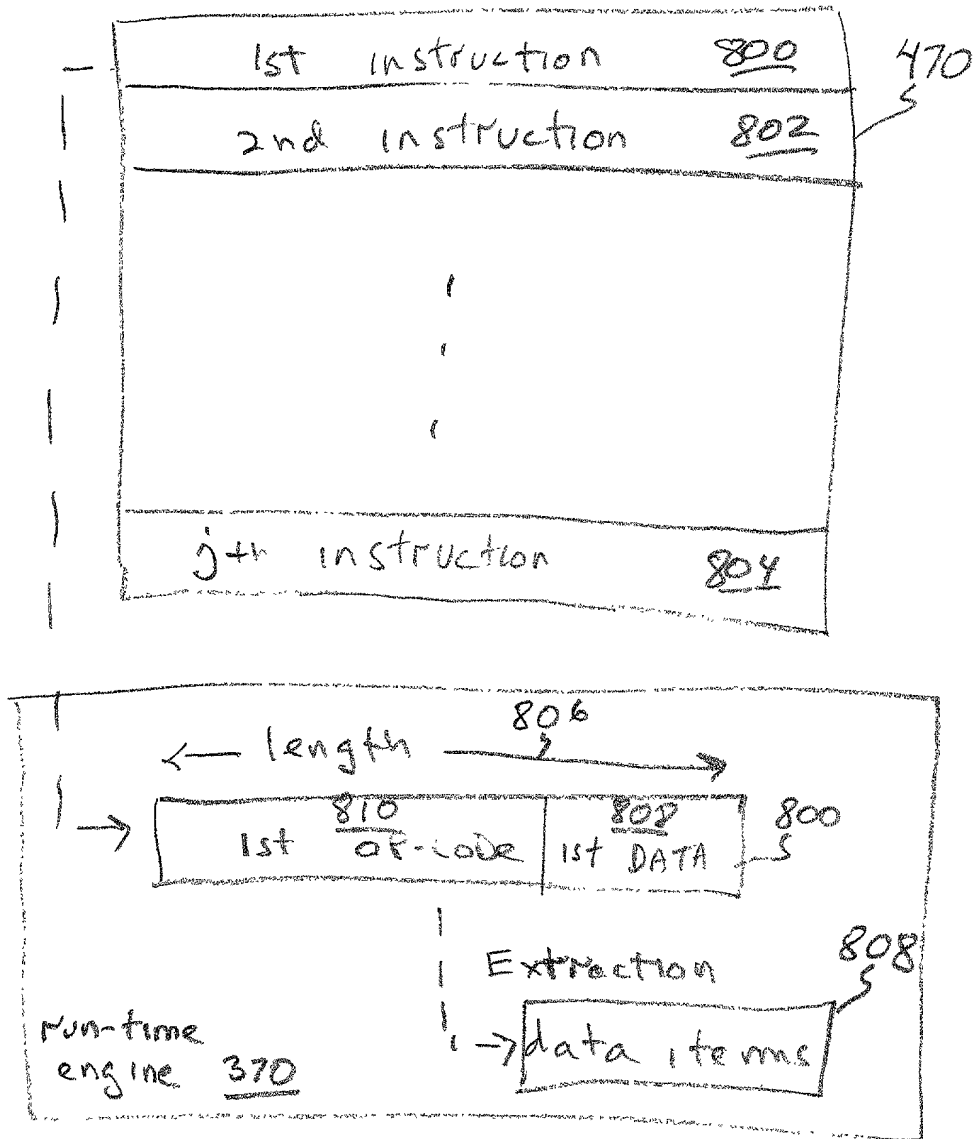


Fig. 8

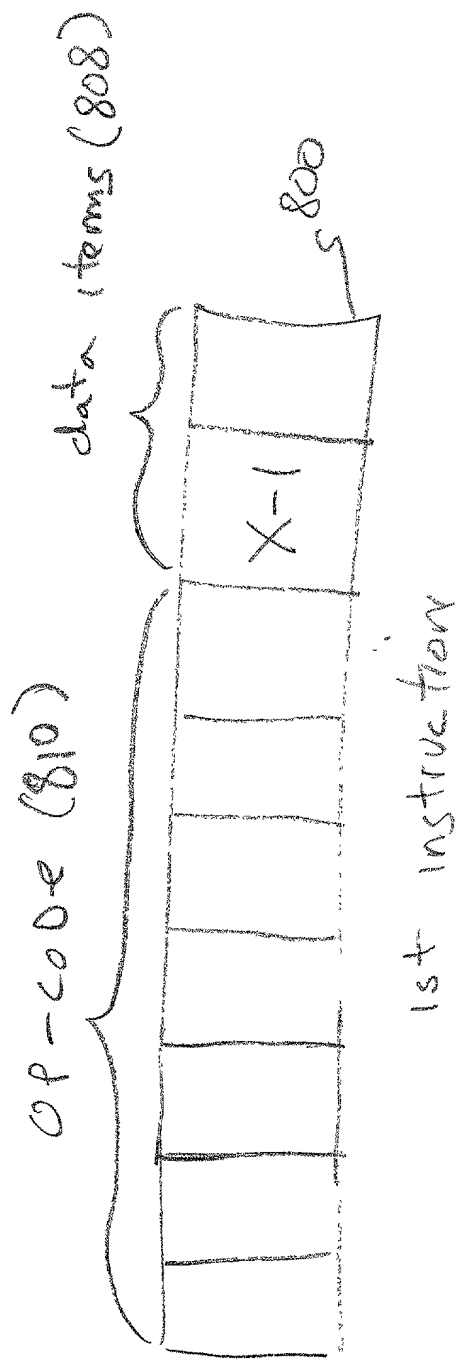


Fig. 9

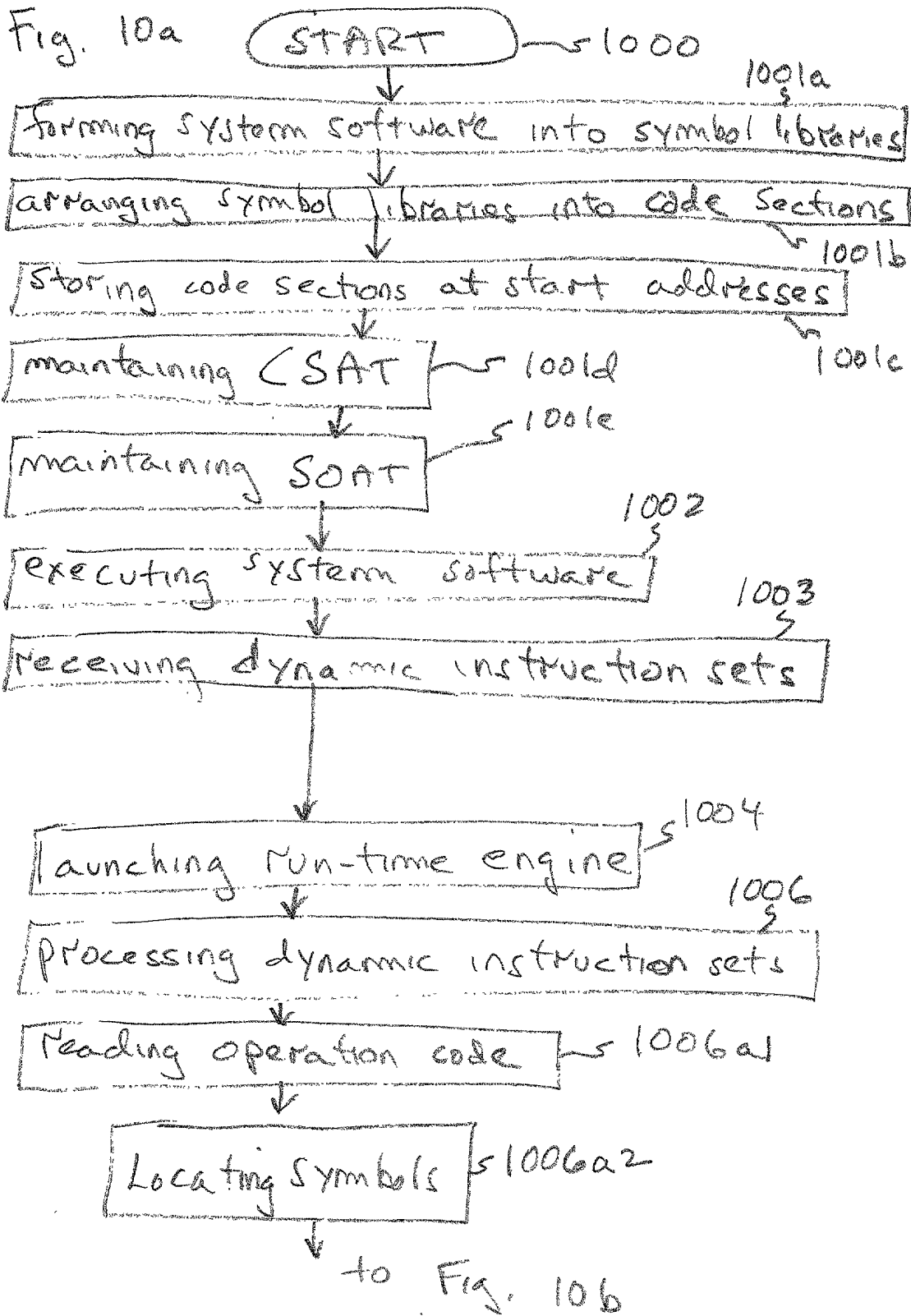


FIG. 10a

Fig. 11

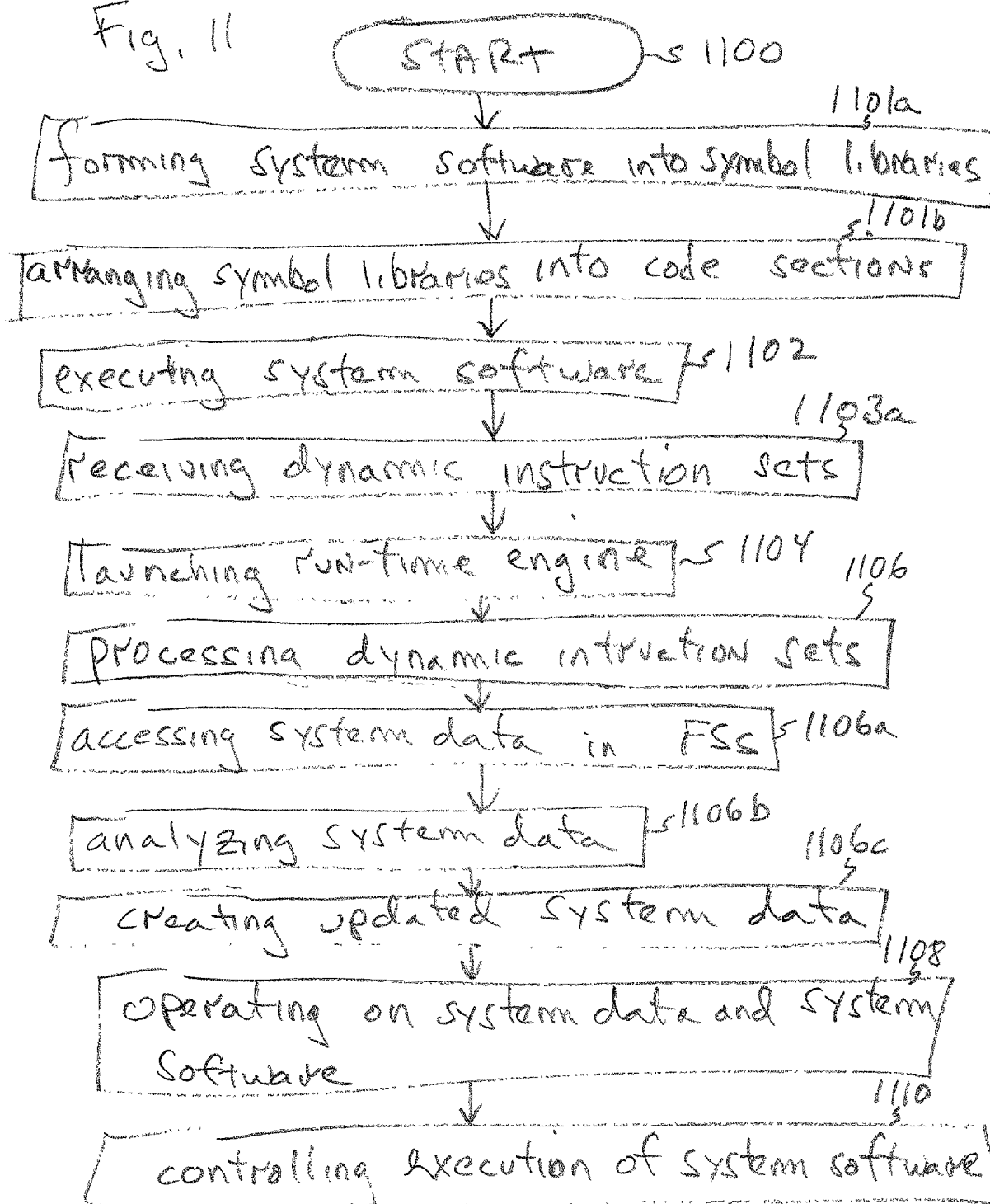
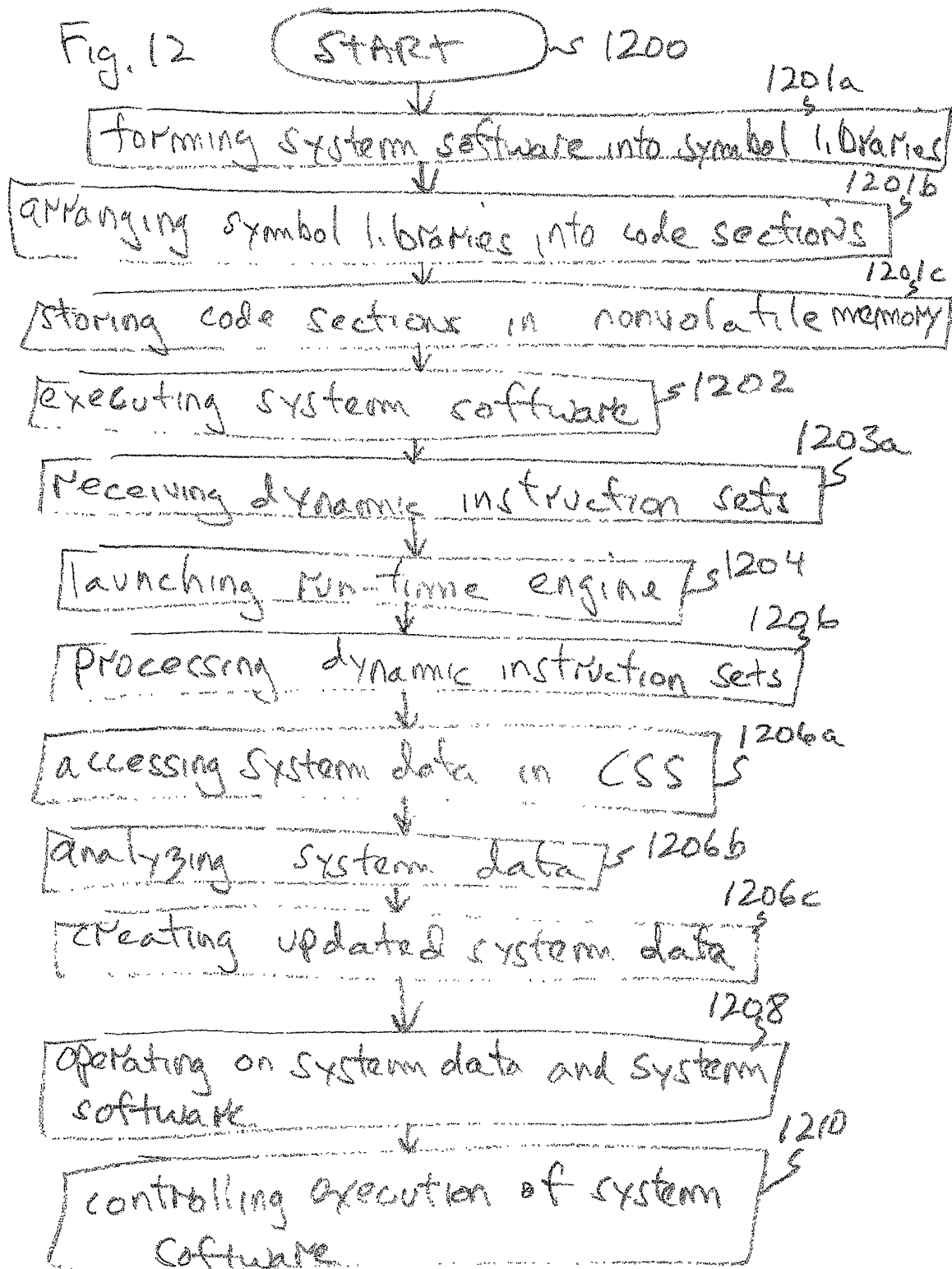


Fig. 12



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Fig. 13

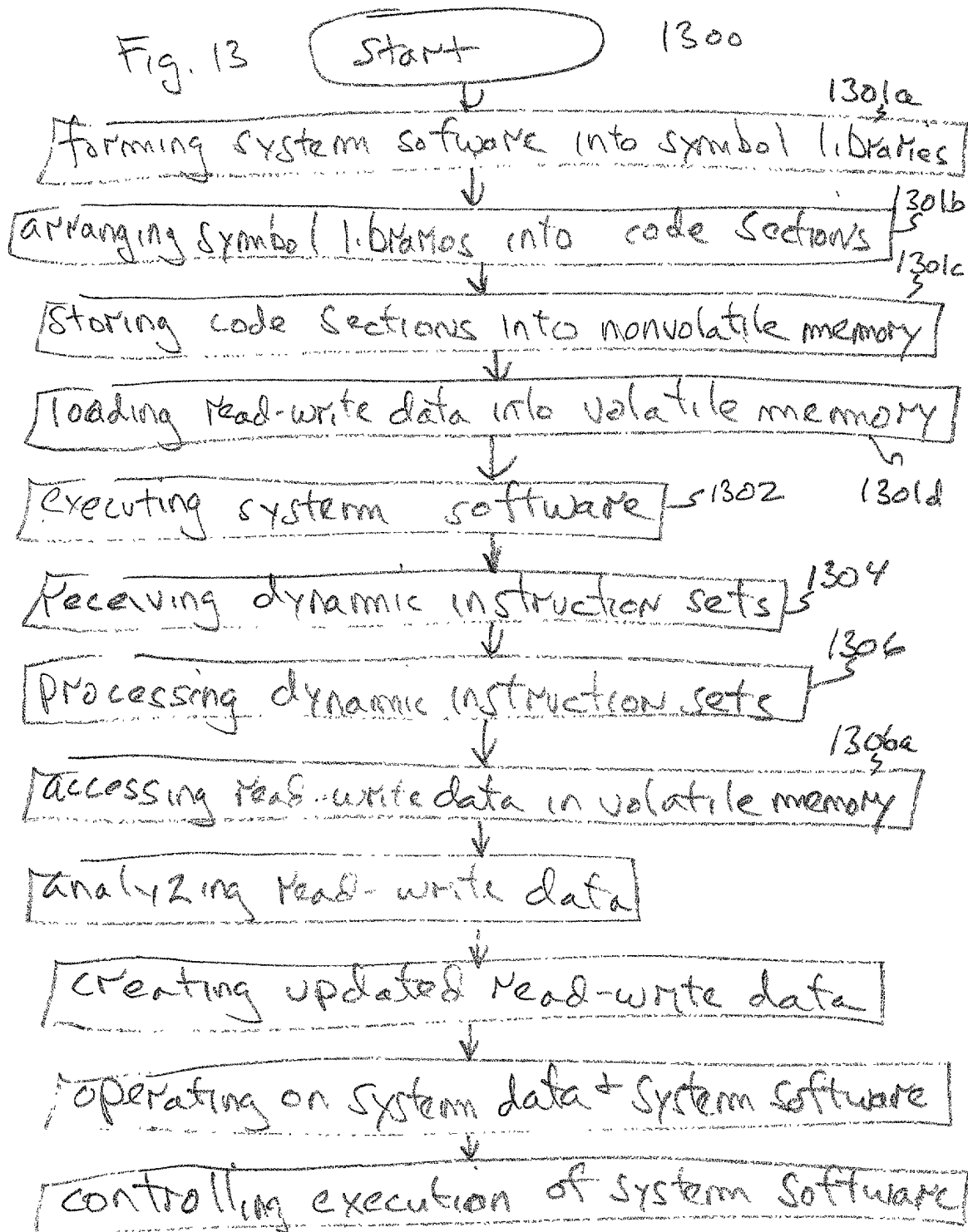


Fig. 14

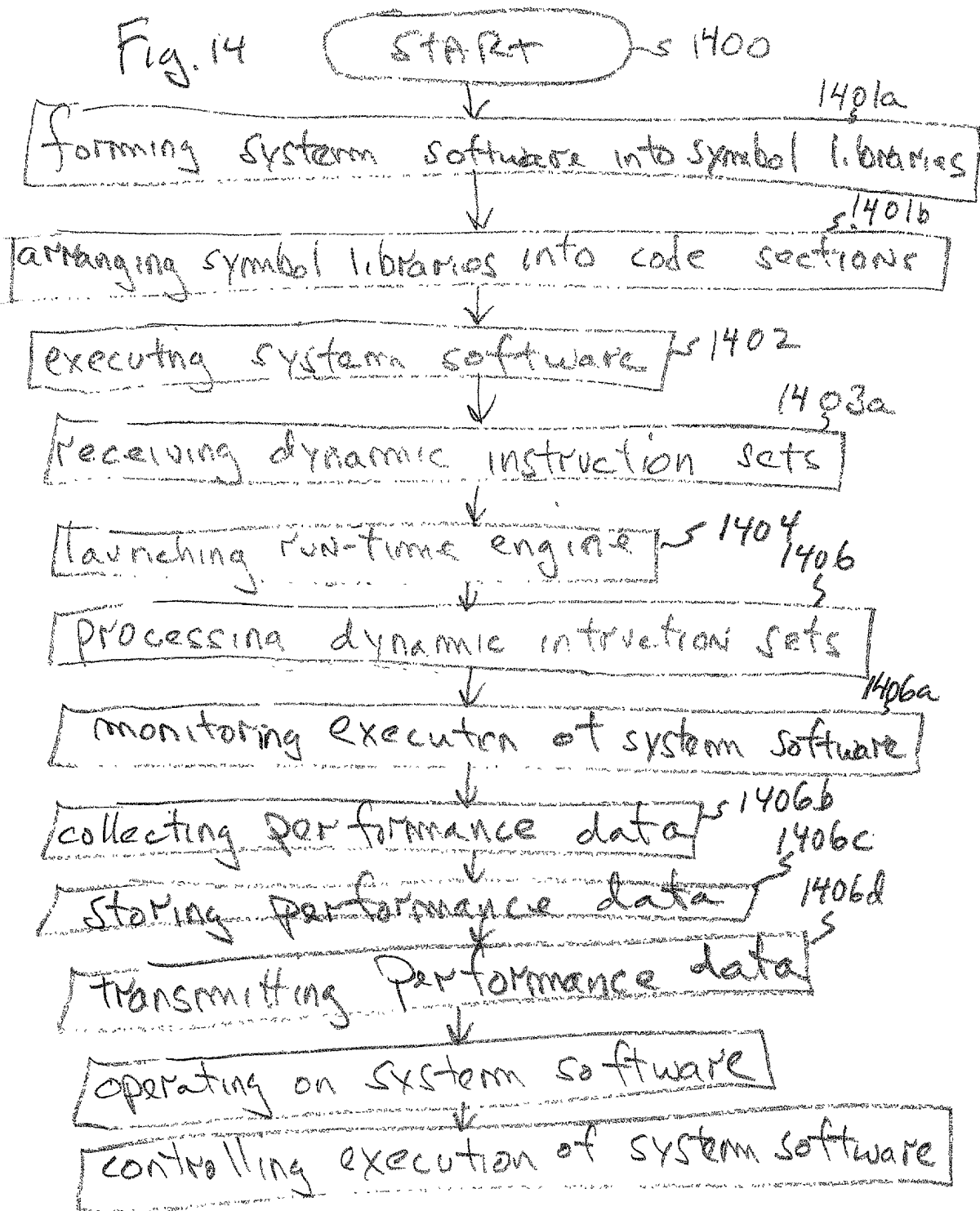
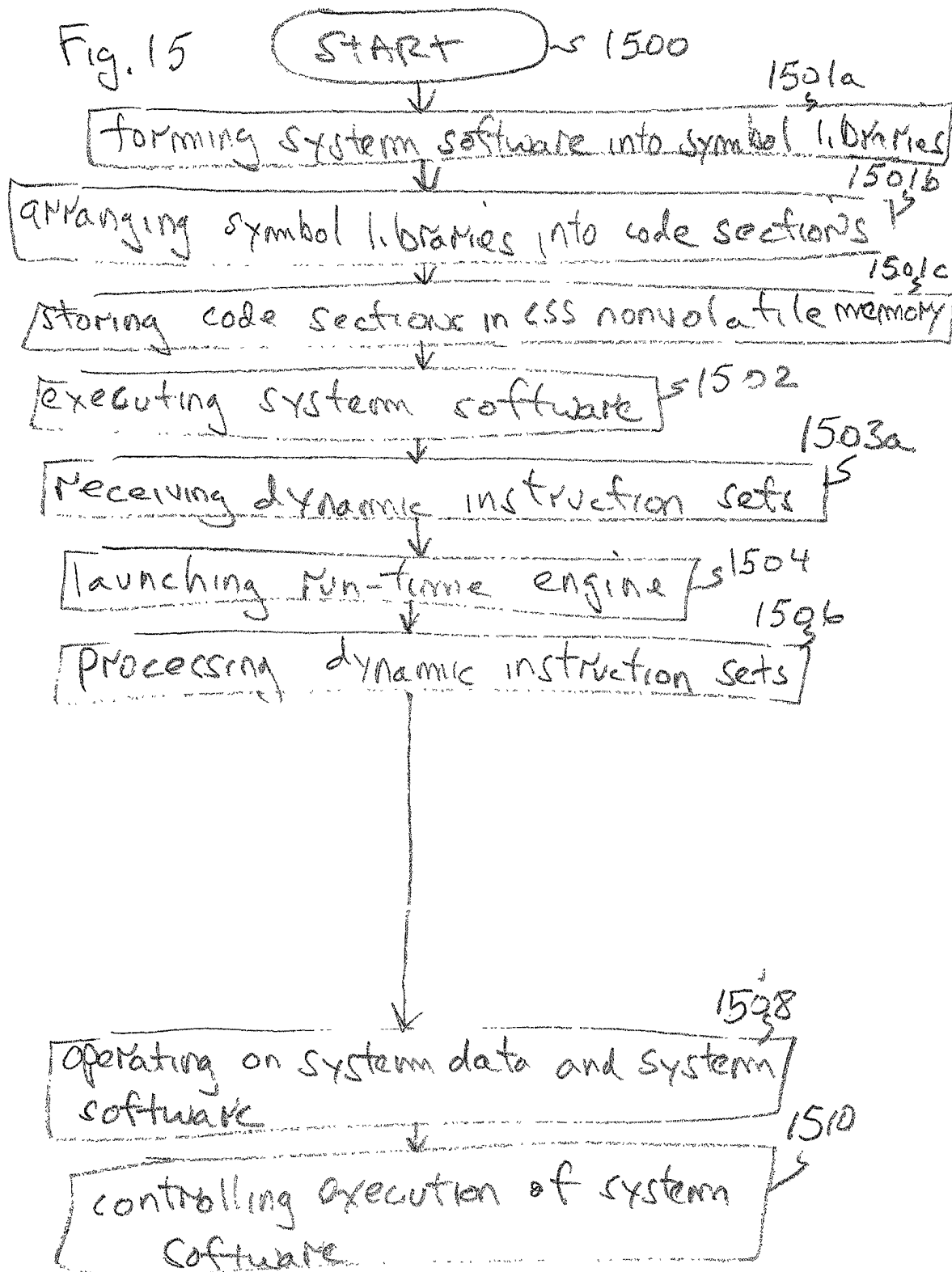


Fig. 15



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